REMARKS

The Official Action mailed May 25, 2005, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicants respectfully submit that this response is being timely filed.

The Applicants note with appreciation the consideration of the Information Disclosure Statements filed on June 17, 1999, May 30, 2000, October 4, 2000, September 26, 2001, March 13, 2002, April 30, 2003, June 17, 2003, April 6, 2004, and August 23, 2004. A further Information Disclosure Statement was filed on June 10, 2005 (received by OIPE June 15, 2005). The Applicants respectfully request that the Examiner provide an initialed copy of the Form PTO-1449 evidencing consideration of the Information Disclosure Statement filed June 10, 2005.

Claims 1, 2, 11-14, 16, 38-41, 58, 59, 71, 72, 78, 79, 100, 101 and 122-145 are pending in the present application, of which claims 1, 2, 122, 128, 134 and 140 are independent. Claims 1 and 2 have been amended to correct minor informalities. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 1 of the Official Action objects to claims 1, 2, 11-14, 16, 38-41, 58, 59, 71, 72, 78, 79, 100, 101 and 122-145 for informalities or defects. As the objection is best understood, it appears the Official Action is asserting that a hypothetical interpretation of claims 1, 2, 122, 128, 134 and 140 is not supported by the specification and Figures. However, it is noted that the claims are read in light of the specification, and a hypothetical interpretation of the claims cannot be the basis of a rejection asserting a lack of support in the specification. Also, it is respectfully submitted that the specification provides sufficient support for the broadest reasonable interpretation of the claims. For example, Figure 3 and the associated descriptions in the present specification provide clear support for channel-forming regions of at least two transistors separately provided in at least two separate semiconductor layers respectively. The

Applicants respectfully submit that claims 1, 2, 11-14, 16, 38-41, 58, 59, 71, 72, 78, 79, 100, 101 and 122-145 are adequately described in the specification. Accordingly, reconsideration and withdrawal of the objections are in order and respectfully requested.

Paragraphs 3 and 4 of the Official Action reject claims 1, 2, 11-14, 16, 38-41, 58, 59, 71, 72, 78, 79, 100, 101 and 122-145 as obvious based on the combination of U.S. Patent No. 5,589,406 to Kato et al., EP 0 502 749 to Yamazaki et al. and/or U.S. Patent No. 5,173,792 to Matsueda, either alone or in combination with U.S. Patent No. 5,403,772 to Zhang et al. The Applicants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

There is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify Kato and

EP '749 and/or Matsueda or to combine reference teachings to achieve the claimed invention. MPEP § 2142 states that the examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. It is respectfully submitted that the Official Action has failed to carry this burden. While the Official Action relies on various teachings of the cited prior art to disclose aspects of the claimed invention and asserts that these aspects could be used together, it is submitted that the Official Action does not adequately set forth why one of skill in the art would combine the references to achieve the features of the present invention.

Kato is relied upon to allegedly teach "an active matrix type LC device having a buffer circuit in the drive circuit ... comprising: a first TFT (the middle one of 10D1(i)) and second TFT (the lower one of 10D1(i)) ... formed in separated portions of a Si layer" (page 3, Id.). The Official Action concedes that Kato does not teach "that the two parallel-connected TFTs can be arranged in the channel width direction" (page 3, Paper No. 20050523). The Official Action relies on EP '749 and/or Matsueda to allegedly teach semiconductor layers arranged in a channel width direction. The Official Action asserts that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the TFT device of Kato with the parallel-connected TFTs being arranged in the channel width direction, per the teachings of EP '749 and/or Matsueda, so that a TFT device with another common parallel connection layout for the parallel-connected TFTs and/or with a TFT parallel connection layout that is tighter, simpler, and/or more straight forward, would be obtained" (page 4, Id.). The Applicants respectfully disagree and traverse the above assertions in the Official Action.

Although EP '749 and Matsueda appear to teach semiconductor layers arranged in a channel width direction, the semiconductor layers of EP '749 and Matsueda are related to pixel portions of a display device and are not related to a buffer circuit or a driver circuit. The Official Action has not shown why one of ordinary skill in the art at the time of the present invention would have been motivated to apply features of the

semiconductor layers associated with pixel portions of a display device in EP '749 and/or Matsueda to the column-drive-TFTs 10Dx of Kato.

Further, the Applicants note that similar arguments were made in the *Appeal Brief* filed January 13, 2004 (e.g., pages 8-10). As a result, the rejections based on Matsueda were withdrawn.

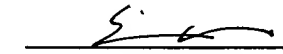
Zhang does not cure the deficiencies in Kato, EP '749 and Matsueda. Zhang is relied upon to allegedly teach a monocrystalline semiconductor layer (pages 4-5, Paper No. 20050523). Zhang does not teach or suggest why one of ordinary skill in the art at the time of the present invention would have been motivated to apply features of the semiconductor layers associated with pixel portions of a display device in EP '749 and/or Matsueda to the column-drive-TFTs 10Dx of Kato.

In the present application, it is respectfully submitted that the prior art of record, either alone or in combination, does not expressly or impliedly suggest the claimed invention and the Official Action has not presented a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

For the reasons stated above, the Official Action has not formed a proper *prima facie* case of obviousness. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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